

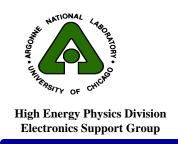
Argonne National Laboratory High Energy Physics Division Electronics Support Group

Long Range Planning Presentation

Current Projects, Capabilities, and New Initiatives

Presented By

Gary Drake Dec. 2, 2003



Group Personnel

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• Gary Drake Group Leader, EE

• John Dawson Senior EE (part-time)

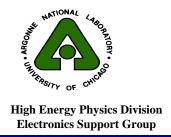
• Bill Haberichter Engineering Specialist

• Tim Cundiff Engineering Assistant

• Leon Reed Engineering Assistant

(part-time)

Carolyn Adams Technician



Group Specialties and Expertise

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A. Design of High-Speed Data Processors

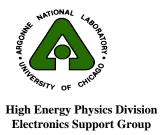
Types of Projects:

- Trigger Processors
- Communication Interface
- Data Acquisition



Implementation Techniques:

- Multi-Layer Printed Circuit Board Design
- Programmable Logic Devices (PLD)
- Field Programmable Gate Arrays (FPGA)
- Surface Mount Technology
- Ball Grid Arrays (BGA)



Group Specialties and Expertise

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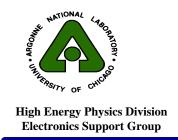
B. Front End Design

- Types of Projects:
 - Charge Amplifiers
 - Preamplifiers
 - Digitizers
 - Discriminators
 - Implementation of Custom Circuits (ASICS)
 - Noise Measurement,
 Analysis, & Abatement
 - HV Power Supply Design

Implementation Techniques:

- Printed Circuit Board Design
- Surface Mount Technology
- Custom Circuit Design (with FNAL)
- Bare Die or Chip on Board (COB)





Group Specialties and Expertise

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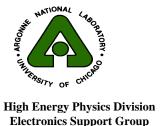
C. System Design

- Types of Projects:
 - Trigger Systems (CDF, ATLAS, ZEUS)
 - ◆ Front End System for Shower Max (CDF)
 - Front End System for Calorimetry (MINOS, LC)
 - Front End System for Tracking (ZEUS)
 - » Often, These Projects Are Leadership Roles...

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A. CDF Shower Max Front End Electronics - Run II

- Activities & Status
 - Project Engineer
 - Responsible for Design of Overall System
 - Coordination of Engineering Activities, ANL & FNAL
 - Sub-component Design and Production
 - *SMXR* (VME Read-Out Board) 100 Boards
 - *SQUID* (Host PCB for Front-End Custom ASIC) 5000 Boards
 - *Preamp* for Strip & Wire Chambers 12,000 SIPs
 - ◆ Status
 - Completed Production in Spring 2001 **>> Working Well to Date**
 - Currently Providing Maintenance & Support for Entire System



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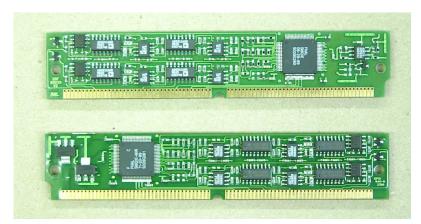
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A. CDF Shower Max Front End Electronics (Cont.)

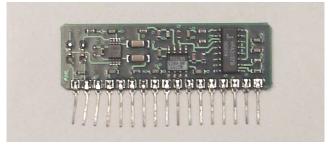
Gallery of Our Designs



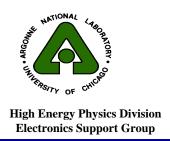
SMXR



SQUID



CES Preamp

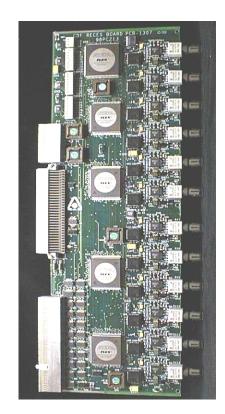


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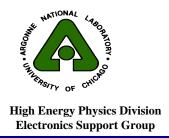
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A. CDF Trigger Electronics – Run II

- Activities & Status
 - ◆ Isolation Trigger
 - Level 2 Trigger for Isolated Photons
 - * RECES
 - Level 2 Trigger for Shower Max
 - ◆ Status
 - Completed Production in Spring 2001
 - Currently Providing Maintenance & Support



RECES Board

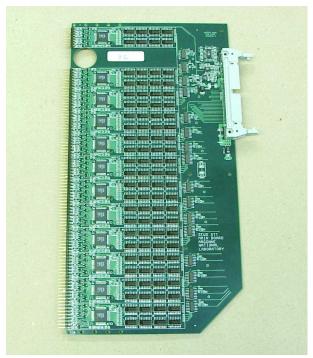


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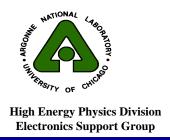
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C. ZEUS Straw Tube Tracker (STT) Electronics

- Design and Production of the Main Board
 - Discriminator Board for Processing Straw Tube Signals
 - ◆ Front End Board Hosts the *ASDQ*, A Custom Front End Chip Designed at PENN
 - ◆ Low-Noise, High Sensitivity (2 fC)
 - 150 Boards for Production
 - Status: Completed Spring, 2001



» High Density Layout, Low Noise Performance, Mixed Analog/Digital Circuitry



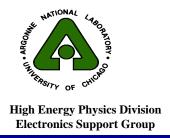
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C. ZEUS Straw Tube Tracker Electronics (Cont.)

- Design of the Driver Board
 - ◆ Board for Driving Discriminated Signals~42 M from Detector to Counting Room
 - Contains 16 Driver Amplifiers
 Configured as SIPs
 - Compensates for Lossy Cable
 - ◆ 150 Boards for Production
 - Designed at ANL
 - Production and Checkout Done at Tel Aviv Univ.
 - Status: Production Completed Spring, 2001



» Novel Amplifier for Compensating Lossy Cable



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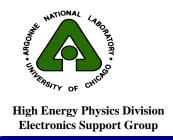
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D. ZEUS Cockroft-Walton Photomultiplier Base

- Design and Production of the CW PMT Base
 - ◆ PMT Base with Internal High Voltage Generation from Low Voltage DC
 - ◆ Low Power, Low-Noise, with Monitor Read Back
 - Replacement for Existing Failing Bases
 - ◆ 500 (1000) Boards for Production
 - Designed at ANL
 - ◆ Production and Checkout Done at Penn State Univ.
 - ◆ Status: Production of 500 Completed in Spring, 2001 → Working Well to Date



» Low Noise, High Density, Unique Packaging, Reliability



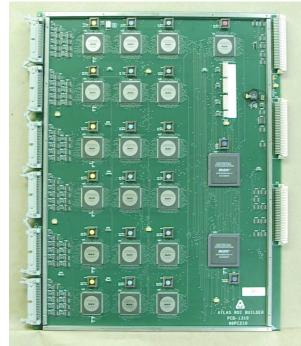
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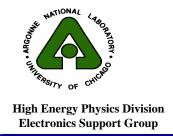
E. ATLAS Level 2 Trigger

• Design of the Region of Interest (ROI) Builder

- Receives Information from Level 1 Trigger,
 Forms a "Record," and Passes it to the
 Trigger Supervisor for L2 Processing
- High Speed, High Bandwidth, High Density
- ◆ Have Demonstrated Ability to Meet 100 KHz Maximum Output Trigger Rate
- ◆ Status: 1st Prototype Built, & Tested at CERN; Design of Final Prototype in Progress
- ◆ Schedule: Production ~2004



» Extensive Use of High Density Programmable Logic



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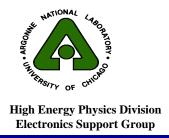
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F. ATLAS Communication Link

- Design of the TTC Mezzanine Card
 - Hosts TTCrx Custom Chip, Developed at CERN
 - ◆Timing and Control Information from Master Clock (TTC), Transmitted over Fiber to All Parts of Detector
 - High Speed, High Bandwidth, High Density
 - ◆ Uses Ball Grid Array (BGA) Technology
 - ◆ Status: 4 Prototypes Tested in ATLAS Tilecal Testbeam; Other Testing in Progress
 - ◆ Schedule: Evaluation in Progress...



» High Density Programmable Logic, BGA Packaging



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G. ATLAS Communication Link

- Design of the Gigabit Ethernet Link-Source Card
 - ◆ Receives "S-Link" Input Data Streams
 - ◆ Buffers Data, & Re-Transmits over Gigabit Ethernet Fiber
 - ◆ Interface Between L1 & L2 Trigger Systems
 - High Speed, High Bandwidth, High Density
 - Status: Prototypes Built;
 Testing in Progress at CERN
 - ◆ Schedule: Production ~2004

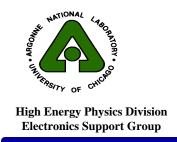


» Extensive Use of High Density Programmable Logic, Complex Functionality

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H. MINOS Near Detector Front End System

- Level 3 Manager for Near Detector Electronics
 - Responsible for Design of Overall System
 - Coordination of Subproject Engineering Activities
 - Design & Production Joint Effort with ANL, FNAL, & IIT



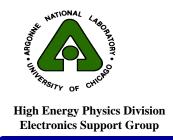
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H. MINOS Near Detector Front End System (Cont.)

- Design and Production of the MASTER Module
 - High-Speed Front End Data Processor
 - 9U x 400mm VME Board
 - 100 Boards for Production
 - Checkout Performed at ANL
 - Status: Production in Progress
 - Schedule: Complete January 2004



» Extensive Use of High Density Programmable Logic, Complex Functionality



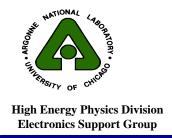
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H. MINOS Near Detector Front End System (Cont.)

- Design and Production of the MINDER Module
 - Motherboard for Front End Electronics Channels
 - Host to Daughter Boards
 Containing *QIEs*, A Custom Front
 End Chip Designed at FNAL
 - 6U x 340mm VME Board
 - ◆ 700 Boards for Production
 - Checkout Performed at ANL
 - Status: Production in Progress



» High Density Programmable Logic, Mixed Analog/Digital Processing, Low Noise



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H. MINOS Near Detector Front End System (Cont.)

- Design and Production of the KEEPER Module
 - Controller for Front End Crates
 - Contains Discriminators for PMT Dynodes for Triggering
 - 6U x 340mm VME Board
 - 55 Boards for Production
 - Checkout Performed at ANL
 - Status: Production in Progress
 - Schedule: Complete



» High Density Programmable Logic, Mixed Analog/Digital Processing, Low Noise

New Projects (With Funding)

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A. Linear Collider

- Readout System for Hadron Calorimeter
 - Detector Technology: Resistive Plate Chambers
 - Project: Design Readout System for Prototype Detector
 - Overall Front-End Electronics & DAQ
 - Specification of Custom Integrated Circuit (Design at FNAL)
 - Coordination of Design Activities
 - Prototype Design, Development, & Testing
 - Cockroft-Walton HV
 - ◆ Design & Production Joint Effort with ANL, FNAL, U of C, & Boston University

New Projects (With Funding)

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B. NUMI Off-Axis Experiment

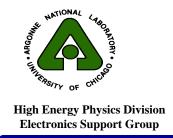
- Readout System for Calorimeter
 - Detector Technology: Resistive Plate Chambers (Scintillator?)
 - Project: Design Readout System for Detector
 - Overall Front-End Electronics & DAQ
 - Specification of Custom Integrated Circuit (Same as LC...)
 - Coordination of Design Activities
 - Prototype Design, Development, & Testing
 - Cockroft-Walton HV
 - ◆ Design & Production Joint Effort with ANL & FNAL (and LC...)

New Projects (With Funding)

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C. Veritas

- Readout System for Upgraded Telescope
 - Detector Technology: Mult-Anode PMTs
 - Project: Design Readout System for Prototype Detector
 - Evaluation of MAPMTs for Telescope
 - Overall Front-End Electronics & DAQ
 - Prototype Design, Development & Testing
 - Trigger System?



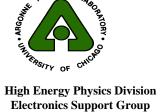
Future Projects

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Projects We Are Discussing:

- Front End Electronics for *OMNIS*
- L2 Upgrade for *CDF Run IIB*
- Front End Electronics for *Reactor Neutrino Experiment*



Group Personnel Revisited

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Expertise By Discipline	System Design	Digital Design	Prog. Logic Design	Analog Design	Ana/Dig PCB Design	Ground, Shield, & Noise	FE Pwr System Design	Custom IC Design	Checkout, Building, Testing	Comp. Program Support
Dawson (Engineer)	**	*	\uparrow				\(\)			
Drake (Engineer)	\rightarrow			*	\rightarrow	\rightarrow	**	(**)		
Cundiff (Eng. Asst.)					*				**	
Haberichter (Eng. Spec.)		**	*						**	
Reed (Eng. Asst.)									*	
Adams (Tech)				- Support -					*	

Manpower Projection

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• FY2004:

- Support of CDF & MINOS
- Development of ROI Builder & Peripherals for ATLAS
- R&D for (Funded) LC, Veritas, & NUMI Off-Axis
- **» Sufficient Work for Entire Group + Programmer**

• FY2005:

- Support of CDF & MINOS
- Production of ROI Builder for ATLAS (?)
- Production of Electronics for LC Testbeam
- Continued R&D for Veritas, & NUMI Off-Axis (Funding?)
- » Sufficient Work for Entire Group

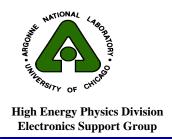
Manpower Projection

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• Beyond FY2005:

- Support of CDF & MINOS
- Support of ROI Builder for ATLAS
- LC: What's Next?
- Veritas & NUMI Off-Axis: Do They Take Off?
- » Staffing Requirements Dependent on New Initiatives



Summary

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We Are Supporting:

- CDF Shower Max Electronics
- CDF Trigger Electronics
- ZEUS STT Electronics
- ZEUS CW PMT Base

Current Active Projects:

- Production of MINOS ND Front End Electronics
- Development of ATLAS ROI Builder
- Development of ATLAS TTC Mezzanine Card & LSC

New Active Projects:

- Linear Collider HCAL
- NUMI Off-Axis FEE
- VERITAS FEE

Future Projects:

- OMNIS FEE
- CDF Run IIB L2 Trigger
- Reactor Neutrino FEE